GW12-500-USR Product Brief

Ultra-short reach SerDes with 500 Gbit/s througput

Overview

The Glasswing SerDes family is a set of programmable IPs designed and optimized for in-package applications. Glasswing provides high system bandwidth with low power consumption through the use of CNRZ-5-DR-EE Chord signaling and a forwarded clock architecture. Deploy Glasswing IP in multiple instances to provide efficient extended interfaces.

Benefits

- x2 to x4 throughput at 50% less energy consumption compared to conventional SerDes over the same number of pins/wires
- High pin-efficiency and low power
- 208.3 Gbit/s full-duplex bandwidth per mm of die edge (500 Gbit/s for 2.4mm of die edge)
- Supports up to 6 dB channel insertion loss at 12.5 GHz
- NRZ-like ISI and noise performance

Technology

- GlobalFoundries® 12LP process
- 0.9V and 1.2V analog supplies
- 0.8V digital supply
- Junction temperature -40 to +110 °C
- Standard flip chip technology with 150 µm bump pitch
- Tile-able layout to support high IO density

Features

- MCM interface consisting of four 6-wire CNRZ-5 Chords, plus a shared forwarded clock (26 wires total per direction)
- No silicon interposer required due to standard 150 µm bump pitch
- Maximum throughput of 500 Gbit/s in each direction
- Lane rate programmable from 12.5 to 25 GBd for a throughput of 62.5 to 125 Gbit/s per Chord
- Total throughput configurable by selecting number of active Chords
- TX and RX data buses consisting of five 32-bit data words (plus clock) for each Chord
- Simple word-based TX to RX interface, RX logic recovers data alignment
- DC-coupled link with no coding/framing requirements; light-weight scrambler in PMA Soft IP ensures sufficient data toggling
- Configuration and link start-up through APB (ARM Peripheral Bus) interface
- Internal TX to RX loopback for wafer/die level test
- Configurable Bolt-On PMA soft IP for ease of use:
  - Scrambler
  - Bit error injection
  - Single cycle FEC to decrease BER/increase link length
  - Option to include PRBS to test impact on BER using FEC
  - Far-end loopback
- RX CTLE equalization for up to 6 dB channel loss at 12.5 GHz
- TX PLL with reference clock input frequency from 100 MHz to 312.5 MHz (25 MHz supported for Test)
- Supports JTAG boundary scan (1149.1) and scan test modes (Shift/Capture and Bypass)
- Integrated diagnostics: PRBS-15 and PRBS-31 pattern generation and verification, RX EyeScope
- DFT: at-speed BIST of analog plus stuck-at scan (Capture and At-Speed)
- ATPG support
- JEDEC JESD247 Multi-wire Multi-level Interface Specification compatible

Applications

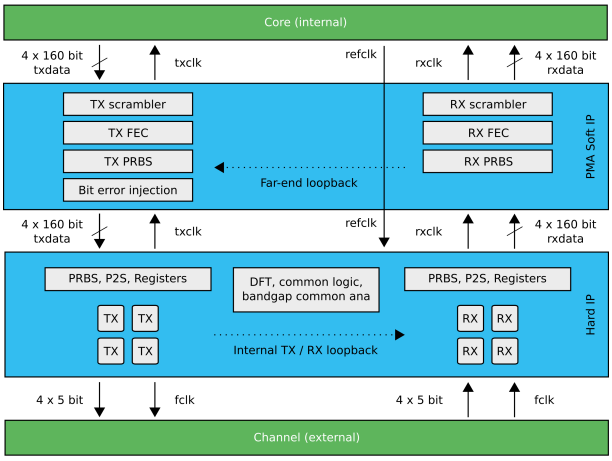
- Multi-chip modules and short reach interposers:
  - Packaging dies with dissimilar foundry processes
  - Packaging of smaller dies to increase yield
- High throughput data interfaces:
  - Efficient interface to off-board SerDes tiles
  - Interconnection of tiled CPUs or DSPs
  - Processor or switch to high bandwidth memory
  - Efficient interface to optics engines
  - Switch-to-switch links

CNRZ coding

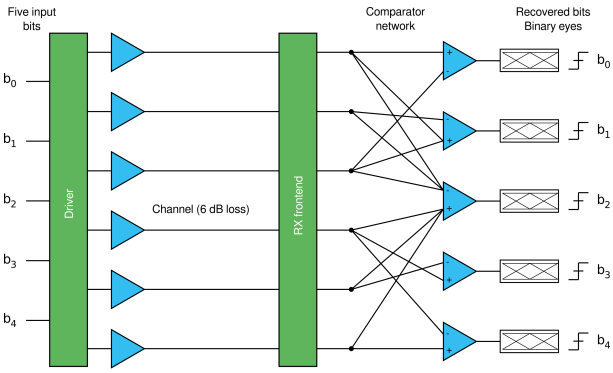
- Transmits 5 bits on 6 correlated wires:
  - Balanced code leads to low SSO noise at transmitter
  - Employs a reference-less receiver that is resilient to common-mode noise
  - Uses a receiver that has five comparators and no decoder
- Link has excellent signal integrity properties:
  - NRZ-like ISI properties
  - Scalable to much higher speeds and harder channels
  - NRZ-like EMI performance

Deliverables

- Datasheet and application notes
- Hard IP standard integration views: LEF, LIB, SDC, GDSII, LVS netlist, ATPG netlist
- PMA Soft IP
- Verilog Hard IP customer model for system simulation; reference test bench
- Qualification report
- Package design and integration guidelines



Block Diagram



Coded Link Block Diagram